REMARKS

Claim Rejections 35 U.S.C. § 112, first paragraph

Claims 26 and 28

The Examiner has rejected claims 26 and 28 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Contrary to the statement by the Examiner, both the specification and the figures do, in fact, describe a via (12) in a passivation layer (13) that is disposed over a bond pad (11B) of a metal line (11A) where the bond pad (11B) is, in turn, disposed over an underlying via (10). See Figure 1b and page 2 of the specification.

Also, see Figure 6f and pages 7-9 of the specification which correspond to a vertical structure, stacked from top to bottom, that includes "bump (25) – segment (24N) of a BLM – via - bond pad - via" from an embodiment of the invention.

In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections to claims 26 and 28 under 35 U.S.C. § 112, first paragraph.

Claim Rejections 35 U.S.C. § 102 (b)

Claims 1, 6-7, and 10-13

The Examiner has rejected claims 1, 6-7, and 10-13 under 35 U.S.C. § 102 (b) as being anticipated by Takeda et al. (JP 05-013418).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 1. Claim 1, as amended, claims a device having Input/Output (I/O) connections including: a bond pad (21B); a passivation layer (23) located over the bond pad; vias (22N, 22N) located in the passivation layer to uncover the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23), the segments connected to the bond pad; and a bump (25) located directly on the segments and in the vias. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

In contrast, the Takeda et al. reference cited by the Examiner teaches a bond pad (3); a final insulating film (4); an aperture in the final insulating film; a second insulating film (5) located in the aperture; vias (unlabeled areas between layers 4 and 5) to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments, the segments in close proximity to each other, the segments separated by a gap, the segments connected to the bond pad; a Cu-plated layer (8) located directly on the segments and in the vias; and a bump (9) located on the Cu-plated layer. See Figure 1 (b).

However, the bump of the Takeda et al. reference is not located directly on the segments. Instead, the Takeda et al. reference teaches an intermediate Cu-plated layer interposed between the BLM and the overlying solder bump.

Furthermore, the bump of the Takeda et al. reference is not located in the vias. Instead, the Cu-plated layer is located in the vias.

Thus, the Takeda et al. reference cited by the Examiner does not teach each and every element of Applicant's invention, as claimed in claim 1, as amended. Consequently, Takeda et al. does not anticipate claim 1, as amended, of Applicant's invention.

Claims 6-7 and 10-13 are dependent on claim 1, as amended, and, thus, are also not anticipated by Takeda et al.

In view of the foregoing, Applicant respectfully requests the Examiner to withdraw the rejections to claims 1, 6-7, and 10-13 under 35 U.S.C. § 102 (b).

Claim Rejections 35 U.S.C. § 103 (a)

Claims 2-4

The Examiner has rejected claims 2-4 under 35 U.S.C. §103 (a) as being unpatentable over Takeda et al. (JP 05-013418) and Tadauchi et al. (US 6,464,122).

Applicant respectfully disagrees with the Examiner. Claims 2-4 are dependent on claim 1, as amended. Claim 2 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump (25) includes a Lead-Tin (Pb-Sn) solder. Claim 3 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump (25) is free of Lead (Pb). Claim 4 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump (25) includes a Tin-Silver-Copper (Sn-Ag-Cu) ternary alloy.

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 1. Claim 1, as amended, claims a device having Input/Output (I/O) connections including: a bond pad (21B); a passivation layer (23) located over the bond pad; vias (22N, 22N) located in the passivation layer to uncover the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23), the segments connected to the bond pad; and a bump (25) located directly on the segments and in the vias. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

In contrast, the Takeda et al. reference cited by the Examiner teaches a bond pad (3); a final insulating film (4); an aperture in the final insulating film; a second

insulating film (5) located in the aperture; vias (unlabeled areas between layers 4 and 5) to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments, the segments in close proximity to each other, the segments separated by a gap, the segments connected to the bond pad; a Cu-plated layer (8) located directly on the segments and in the vias; and a bump (9) located on the Cu-plated layer. See Figure 1 (b).

However, the bump of the Takeda et al. reference is not located directly on the segments. Instead, the Takeda et al. reference teaches an intermediate Cu-plated layer interposed between the BLM and the overlying solder bump.

Furthermore, the bump of the Takeda et al. reference is not located in the vias. Instead, the Cu-plated layer is located in the vias.

Tadauchi et al. teaches a solder containing lead. See Col. 9, line 51.

Thus, a combination of Takeda et al. and Tadauchi et al. would still not produce Applicant's invention, as claimed in claims 2-4. Consequently, Applicant's invention, as claimed in claims 2-4 would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 2-4 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejection to claims 2-4 under 35 U.S.C. §103 (a).

Claims 5 and 8-9

The Examiner has rejected claims 5 and 8-9 under 35 U.S.C. §103 (a) as being unpatentable over Fukuda et al. (JP 05-013418) and Wark et al. (US 6.613,662).

Applicant respectfully disagrees with the Examiner. Claims 5 and 8-9 are dependent on claim 1, as amended. Claim 5 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the bump includes an Electrically

Conductive Adhesive (ECA). Claim 8 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the BLM includes a lower layer and an upper layer and wherein the lower layer includes Titanium (Ti) with a thickness of about200 to 1500 Angstroms. Claim 9 of Applicant's claimed invention claims the device of claim 1, as amended, wherein the BLM includes a lower layer and an upper layer and wherein the upper layer includes Nickel-Vanadium (Ni-V) with a thickness of about 1000 to 8000 Angstroms.

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 1. Claim 1, as amended, claims a device having Input/Output (I/O) connections including: a bond pad (21B); a passivation layer (23) located over the bond pad; vias (22N, 22N) located in the passivation layer to uncover the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23), the segments connected to the bond pad; and a bump (25) located directly on the segments and in the vias. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

In contrast, the Takeda et al. reference cited by the Examiner teaches a bond pad (3); a final insulating film (4); an aperture in the final insulating film; a second insulating film (5) located in the aperture; vias (unlabeled areas between layers 4 and 5) to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments, the segments in close proximity to each other, the segments separated by a gap, the segments connected to the bond pad; a Cu-plated layer (8) located directly on the segments and in the vias; and a bump (9) located on the Cu-plated layer. See Figure 1 (b).

However, the bump of the Takeda et al. reference is not located directly on the segments. Instead, the Takeda et al. reference teaches an intermediate Cu-plated layer interposed between the BLM and the overlying solder bump.

Furthermore, the bump of the Takeda et al. reference is not located in the vias. Instead, the Cu-plated layer is located in the vias.

Wark et al. teaches a bump but does not teach any vias.

Thus, a combination of Takeda et al. and Wark et al. would still not produce Applicant's invention, as claimed in claims 5 and 8-9. Consequently, Applicant's invention, as claimed in claims 5 and 8-9, would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 5 and 8-9 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejection to claims 5 and 8-9 under 35 U.S.C. §103 (a).

Claims 14-15

The Examiner has rejected claims 14-15 under 35 U.S.C. §103 (a) as being unpatentable over Takeda et al. (JP 05-013418) and Wong (US 6,577,017).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 1. Claim 1, as amended, claims a device having Input/Output (I/O) connections including: a bond pad (21B); a passivation layer (23) located over the bond pad; vias (22N, 22N) located in the passivation layer to uncover the bond pad; a BLM (24) located over the vias, the BLM split into two or more segments (24N, 24N), the segments in close proximity to each other, the segments separated by a gap (23), the segments connected to the bond pad; and a bump (25) located directly on the segments and in the vias. See Figures 2a-2b. Also, see lines 17-31 on page 6 and lines 1-4 on page 7 of the specification.

In contrast, the Takeda et al. reference cited by the Examiner teaches a bond pad (3); a final insulating film (4); an aperture in the final insulating film; a second insulating film (5) located in the aperture; vias (unlabeled areas between layers 4 and 5) to uncover the bond pad; a BLM located over the vias, the BLM split into two or more segments, the segments in close proximity to each other, the segments

separated by a gap, the segments connected to the bond pad; a Cu-plated layer (8) located directly on the segments and in the vias; and a bump (9) located on the Cu-plated layer. See Figure 1 (b).

However, the bump of the Takeda et al. reference is not located directly on the segments. Instead, the Takeda et al. reference teaches an intermediate Cu-plated layer interposed between the BLM and the overlying solder bump.

Furthermore, the bump of the Takeda et al. reference is not located in the vias. Instead, the Cu-plated layer is located in the vias.

Wong teaches a single via, but does not teach a bump.

Thus, a combination of Takeda et al. and Wong would not produce Applicant's invention, as claimed in claims 14-15. Consequently, Applicant's invention, as claimed in claims 14-15, would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 14-15 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejection to claims 14-15 under 35 U.S.C. §103 (a).

Claim Rejections 35 U.S.C. § 103 (a)

Claims 26 and 28

The Examiner has rejected claims 26 and 28 under 35 U.S.C. §103 (a) as being unpatentable over Tsuji (JP 08-204136) and Ito et al. (US 5,847,466).

Applicant respectfully disagrees with the Examiner. Applicant has amended claim 26. Claim 26, as amended, claims a device having I/O connections to a

package or board including: vias; a bond pad located over the vias, the bond pad having two or more segments, the segments having the same shape, wherein each of the segments is electrically connected to two or more of the vias, and a wire lead attached directly to the segments. See Figure 5.

However, Tsuji does not teach segments having the same shape.

Thus, a combination of Tsuji and Ito et al. would not produce Applicant's invention, as claimed in claim 26. Consequently, Applicant's invention, as claimed in claims 26, would not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Claim 28 is dependent on claim 26. Thus, a combination of Tsuji and Ito et al. would also not produce Applicant's invention, as claimed in claim 28. Consequently, Applicant's invention, as claimed in claims 28, would also not have been obvious to one of ordinary skill in the art of semiconductor packaging at the time the invention was made.

Since the two references cited by the Examiner do not teach, suggest, or render obvious claims 26 and 28 of Applicant's claimed invention, Applicant respectfully requests the Examiner to withdraw the rejections to claims 26 and 28 under 35 U.S.C. §103 (a).

Conclusion

Applicant believes that all claims pending are now in condition for allowance so such action is earnestly solicited at the earliest possible date.